2588us.doc

PULSE MODULATED DIGITAL TO ANALOG CONVERTER (DAC)

Eran GURESHNIK, Daniel YELLIN, Shlomo YAKOBOVICH and Arie STALBERG

FIELD OF THE INVENTION

The present invention relates to digital to analog converters, in general, and to pulse density modulation (PDM) digital to analog converters, in particular.

BACKGROUND OF THE INVENTION

As part of the ever present drive to reduce the cost, size and power consumption of electronic devices, smaller and simpler components are being used in the design of these devices. Some of these components are driven by analog control signals and require a stable, high-resolution analog control signal in order to work efficiently. The analog control signals are typically produced by digital to analog converters (DACs). In portable cellular telephones, for example, analog control signals are used to determine the working point of a transmission Automatic Gain Control (AGC), which controls the power of an amplifier of a transmitting device. Analog control signals are also used to determine the working point of a voltage-controlled temperature-compensated oscillator (VCTCXO), which is used to modulate the transmitted signal and to demodulate the received signal.

Conventional DACs use various circuits that are known in the art, for example, resistor ladders. Analog circuits such as resistor ladders require a large silicon area when implemented into an integrated complementary metal

oxide semiconductor (CMOS) circuit, a factor which becomes much more significant from a cost perspective when small sub-micron CMOS technology is used.

Digital to analog converters (DAC) based on pulse width modulation (PWM) or pulse density modulation (PDM) methods are known in the art. The PDM method is described in US Patent 5,337,338 to Sutton et al. A pulse modulated DAC comprises a digital circuit which converts a multi-bit digital signal to a single bit digital signal, followed by an analog low pass filter (LPF) which converts the single bit digital signal to a constant level analog signal. The LPF filters out the undesired high frequencies in the single bit digital signal. A simple and economical way to implement a low pass filter is by using one resistor and one capacitor.

The purpose of the analog LPF is to produce a stable analog signal output that is the average of the discrete levels of the single bit digital signal input. One of the disadvantages of the PWM and PDM methods is that the analog signal output is not constant, but rather has an inherent harmonic ripple in it due to the charging and discharging of the capacitor. This ripple adversely affects the analog components controlled by the analog signal output. For example, a ripple imposed onto an AGC modulates the carrier frequency and generates undesired spurious transmission signals. A ripple imposed onto a VCTCXO will generate spurious replicas of the desired transmission signal at multiples of the ripple frequency, and will interfere with the desired received signal. Another disadvantage is that when the pulse modulated signal changes to represent a different multi-bit digital signal, a relatively long response time is required until the LPF output reaches the new desired value. These two

disadvantages are related: trying to reduce the ripple by decreasing the cutoff frequency results in a slower response time.

Various digital to analog converters, using PWM or PDM methods, are described in the US Patents 5,774,084 to Brombaugh et al., 5,764,165 to Buch, 5,712,636 to Buch, and 5,784,019 to Wong et al. US Patent 5,617,060 to Wilson et al. describes an automatic gain control (AGC) and DC offset correction method and apparatus that uses PDM and a conventional low pass filter. US Patent 5,204,594 to Carbolante discloses a circuit for providing a signal proportional to the average current flowing through coils of a motor operated in both linear and PWM modes.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the appended drawings in which like reference characters identify correspondingly throughout and wherein:

Fig. 1 is a schematic illustration of a portion of an integrated circuit having a DAC of a preferred embodiment of the present invention implemented in it;

Fig. 2A is an exemplary graphical illustration of a pulse modulated signal as a function of time;

Figs. 2B, 2C and 2D are exemplary graphical illustrations of the output analog signal of Fig. 1 as a function of time;

Fig. 3 is a schematic illustration of the digital converter of Fig. 1, according to a preferred embodiment of the present invention;

Fig. 4 is an exemplary graphical illustration of pulse modulated digital signals as a function of time; and

Fig. 5 is a schematic illustration of a modified version of the digital converter of Fig. 3, according to a further preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The present invention is directed to a digital to analog converter (DAC) and to methods of operating a digital to analog converter. The DAC of the present invention is small in size due to the small number of analog components and has relatively low power consumption.

Reference is now made to Fig. 1, which is a schematic illustration of a portion of an integrated circuit 100, having a DAC of a preferred embodiment of the present invention implemented in it. Reference is made additionally to Fig. 2A, which is an exemplary graphical illustration of a pulse modulated signal as a function of time, and to Figs. 2B, 2C and 2D, which are exemplary graphical illustrations of the output analog signal of Fig. 1 as a function of time. In Figs. 2B, 2C and 2D, the horizontal line 201 indicates the desired constant analog signal.

The DAC comprises a digital converter 102, a switchable low pass filter (LPF) 104, an amplifier 108 and a buffer 110. The digital converter 102 converts a multi-bit digital signal to a single bit digital signal, for example using pulse width modulation (PWM) or pulse density modulation (PDM) methods to create a pulse modulated signal.

The switchable LPF 104 receives the single bit digital signal and produces an analog signal. The switchable LPF 104 comprises a first switch SW1 connected to a first resistor R1, a second switch SW2 connected to a second resistor R2, a capacitor C connected serially to the resistors R1 and R2, and a controller 106. The resistors R1 and R2 are connected in parallel. The resistance of the first resistor R1 is small relative to the resistance of the

second resistor R2. In a non-limiting example, the resistance of the first resistor R1 is ten times smaller than the resistance of the second resistor R2.

The controller 106 is operative to open and close switches SW1 and SW2, thereby creating one of three modes of operation of the low pass filter 104.

a) Fast response – large ripple mode

When the switch SW1 is closed and the switch SW2 is open, the low pass filter formed by the resistor R1 and the capacitor C has a fast response time T_1, and a large ripple in the steady-state. This is shown in Fig. 2B by the solid line graph 200 As is known in the art, the ripple frequency coincides with the pulse frequency.

b) Slow response – small ripple mode

When the switch SW1 is open and the switch SW2 is closed, the low pass filter formed by the resistor R2 and the capacitor C has a slow response time T_2, and a small ripple in the steady-state. This is shown in Fig. 2B by the dotted-line graph 202. As is known in the art, the ripple frequency coincides with the pulse frequency.

c) Hold mode

When both the switches SW1 and SW2 are open, the capacitor C is in hold mode, and its voltage level remains almost steady, decreasing slowly in time due to parasitic leakage and leakage through the resistors and switches. This is shown in Fig. 2B by the flat dashed line 204.

According to a preferred embodiment of the present invention, the DAC achieves a fast response time and a small ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the

controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2C by the solid-line graph 206. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2C by the dotted-line graph 208. In such a way, the DAC takes advantage of the fast response mode while the capacitor C is charging, and takes advantage of the small ripple mode when the capacitor C is close to or already at the desired voltage level. As a result, the DAC of the present invention produces a far more stable analog control signal than that of a conventional pulse modulated DAC.

Amend A6 According to another preferred embodiment of the invention, the DAC achieves a fast response time and no ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2D by the solid-line graph 210. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2D by the dotted-line graph 212. When a no-ripple, very stable analog signal is required at beginning at time T_3, the controller 106 opens both switches SW1 and SW2 so that the capacitor C will retain its voltage level in hold mode. This is shown in Fig. 2D by the almost flat dashed line 214.

Amend A7 The motivation for this preferred embodiment is that there are cases, such as control signals for time division multiple access (TDMA) applications,

where a very stable, slowly decreasing signal is preferable to even a small ripple. In such applications, the controller is set so that the time T_3 precedes or substantially coincides with the time at which the analog control signal is needed.

A further advantage of this preferred embodiment is that during hold mode, the switchable LPF 104 draws no current, and the digital converter 102 can be turned off, resulting in a reduction in the overall power consumption.

It will be appreciated that the controller 106 may close both switches SW1 and SW2 when a particularly small resistance is desired.

The operation of the digital converter 102 of Fig. 1 will now be explained with respect to Figs. 3 and 4, to which reference is now made. Fig. 3 is a schematic illustration of a pulse density modulation (PDM) digital converter, according to a preferred embodiment of the present invention.

The digital converter 102 comprises an adder 302 and a flip-flop 304. Initially, the flip-flop has a value of 0. With each cycle of a clock 306, the adder 302 adds the N-bit digital signal input, which is a number having a value between 0 and 2^{N-1}, to the value stored in the flip-flop 304. When the adder 302 reaches or passes the value 2^{N-1}, a pulse is generated. Any remaining value of the adder 302 beyond 2^{N-1} is sent to the flip-flop 304 to be added in the next clock cycle. In such a way, a signal is generated with pulses whose density is proportional to the N-bit digital signal input. This signal is shown by the solid-line graph in Fig. 4, which is an exemplary graphical illustration of the voltage of the pulse modulated digital signal of Fig. 3 as a function of time.

According to a further preferred embodiment of the present invention, the DAC spreads the spectral properties of the harmonic ripple using random

noise. As is known in the art, a PDM signal is composed of pulses whose density is proportional to the value of the multi-bit digital input signal. The frequency of these pulses, known as the ripple frequency, appears in the output analog signal and interferes with the desired signal. The same problem occurs with the output analog signal of a PWM signal, although its ripple frequency is generally lower than that generated by a PDM signal. In the further preferred embodiment of the present invention, the timing of the pulses in the pulse modulated signal is adjusted by a small, random factor, thereby spreading the spectral properties of the harmonic ripple. Reference is now made additionally to Fig. 5, which is a schematic illustration of a modified version of the digital converter of Fig. 3, according to a further preferred embodiment of the present invention. In addition to the adder 302 and the flip-flop 304, the digital converter 102 comprises a uniform distribution random number generator 500 and an additional adder 502. The random number generator 500, for example a pseudo-random number (PN) generator, which is known in the art, is driven by a clock 504. For each cycle of the clock 504, the random number generator 500 generates a random number in the range –M to +M, where M is significantly smaller than N. The adder 502 adds the random number to the value in the flip flop 304, and the result is added by the adder 302 to the N-bit digital signal input. The resulting pulse modulated signal is shown in Fig. 4 by the dashed-line graph. The effect is that the pulses generated by the digital converter of Fig. 5 are slightly offset in time ("jittered") from the pulses generated by the digital converter of Fig. 3. Sometimes, as in pulse 400, the two signals are coincident, sometimes, as in pulse 402, the jittered signal is early, and sometimes, as in pulse 404, the jittered signal is late. Introducing a

Amd 910 Cancl.

small random noise into the pulse modulated signal spreads the spectral properties of the pulse frequency (which is the ripple frequency of the analog output signal produced by low pass filtering of the pulse modulated signal).

It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. Rather the scope of the invention is defined by the claims that follow: